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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,713	10/14/2003	Paul Arthur Layman	Chaudhry 25-18-8-12-5/075	4836
29391	7590	07/08/2005	EXAMINER	
BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A. 390 NORTH ORANGE AVENUE SUITE 2500 ORLANDO, FL 32801			POMPEY, RON EVERETT	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

6m

Office Action Summary	Application No. 10/684,713	Applicant(s) LAYMAN ET AL.	
	Examiner Ron E. Pompey	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2-11-04, 3-01-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 20, 21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Holloway et al. (US 4,657,628).

Holloway discloses the limitations of:

forming first(or first device) and second(or second device) spaced-apart diffusion regions (208, 210 fig. 4) on a semiconductor layer;

forming a third semiconductor region(or source and drain region of first transistor) (204 fig. 4) over said first diffusion region, wherein said third semiconductor region has an opposite conductivity type than said first diffusion region;

forming a fourth semiconductor region (or source and drain region of second transistor) (206, fig. 4) over said second diffusion region wherein said fourth semiconductor region has an opposite conductivity type than said second diffusion region;

forming a first gate oxide of a first predetermined thickness adjacent said third semiconductor region;

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forming a second gate oxide of a second predetermined thickness adjacent said fourth semiconductor region (the examiner is taking the first and second predetermined thicknesses to be the same);

forming fifth (gate for first transistor) (N1, fig.4) and sixth(or gate for second transistor) (P1, fig. 4) semiconductor regions, each positioned over one of said third and said fourth semiconductor regions, such that said third and said fifth regions are vertically aligned with one of said first and said second regions, and such that said fourth and said sixth regions are vertically aligned with the other of said first and second regions, the resulting structure providing two transistors(col. 14, Ins. 1-12); and

including the additional step of configuring the first and the second device regions, and the first and the second gate regions into a circuit comprising two MOSFETS(circuit picture, fig. 4).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway et al. (US 4,657,628), as applied to the limitations described above, in view of Lin (US 5,502,009).

Holloway does not disclose the claimed limitation(s) of:

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wherein the step of forming the first gate oxide of a first predetermined thickness adjacent the third semiconductor region and the step of forming the second gate oxide of the second predetermined thickness adjacent the fourth semiconductor region comprises:

forming a first gate oxide of a first predetermined thickness adjacent said third semiconductor region;

forming a second gate oxide of said first predetermined thickness adjacent said fourth semiconductor region;

removing said first gate oxide;

forming a third gate oxide of a second predetermined thickness adjacent said third semiconductor region;

forming said third gate oxide of said third predetermined thickness adjacent said fourth semiconductor region; and

wherein the gate oxide thickness adjacent said fourth semiconductor region is the sum of said first predetermined thickness plus said second predetermined thickness.

However,

a. Lin discloses the above claimed limitations regarding:

wherein the step of forming the first gate oxide of a first predetermined thickness adjacent the third semiconductor region and the step of forming the second gate oxide of the second predetermined thickness adjacent the fourth semiconductor region comprises:

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forming a first gate oxide (13, fig. 1A) of a first predetermined thickness adjacent said third semiconductor region (11, fig. 1A);

forming a second gate oxide (13, fig. 1A) of said first predetermined thickness adjacent said fourth semiconductor region (12, fig. 1A);

removing said first gate oxide (fig. 1B);

forming a third gate oxide (14, fig. 1C) of a second predetermined thickness adjacent said third semiconductor region;

forming said third gate oxide (15, fig. 1C) of said third predetermined thickness adjacent said fourth semiconductor region (12, fig. 1C); and

wherein the gate oxide thickness adjacent said fourth semiconductor region is the sum of said first predetermined thickness plus said second predetermined thickness; and

wherein the first and the second field-effect transistors can withstand different gate input voltages as a consequence of the differing predetermined gate oxide thickness in column(s) 1, line(s) 39-67.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Holloway with Lin, because the formation of different thickness gate oxides provide for versatility in transistors that can be formed in one device.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

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The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.


6. Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 26 recites the limitation "said third and said fourth gates" in lines 4 and 5. There is insufficient antecedent basis for this limitation in the claim.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Ron Pompey
AU: 2812
June 28, 2005


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER